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DL7516 USB HOST MP3 DECODER SOC

DL7516 Datasheet

USB Host MP3 Decoder SOC



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1. Overview

A highly integrated SOC for MP3 player, DL7516 integrates MCU, MP3 decoder, USB Host controller, SD/MMC card controller, ADC, audio DAC and an IR decoder in a single chip. Compared with traditional flash-MP3 player DL7516 offers ultra low cost, low power consumption, flexible and more powerful host MP3 player solution.

1.1 Features

- Low power 0.18um CMOS technology
- Enhanced 8051, up to 10 times faster than standard 8051
- USB2.0 full-speed host controller
- SD/MMC card controller
- Support MPEG 1/2/2.5 layer2/3 decoding, data rate 32kbps ~ 320kbps, including VBR
- Support 9 sampling frequency:
8kHz/11.025kHz/12kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz
- Embedded sound equalizer
- Support tag format ID3v1 and ID3v2.4
- Support FAT16/FAT32 file system
- Embedded 16-bit DAC
- 1 channel AUX in
- 1 channel FM in
- 1 channel 6bit SARADC for peripheral controls
- Support IR Remote control
- GPIO for various purposes
- Embedded LDO, convert 5V to 3.3V and 1.8V
- Embedded Power-on-Reset
- Embedded ROM for program code storage



1.2 Chip Architecture

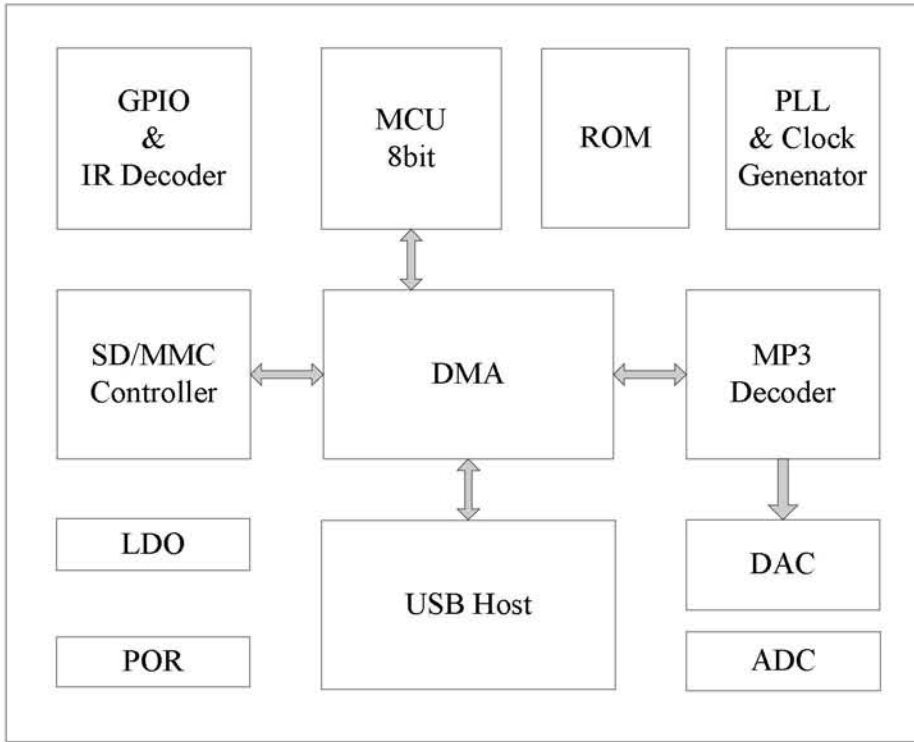


Figure 1 DL7516 Functional Block Diagram

2. System Application

- MP3 mini audio system

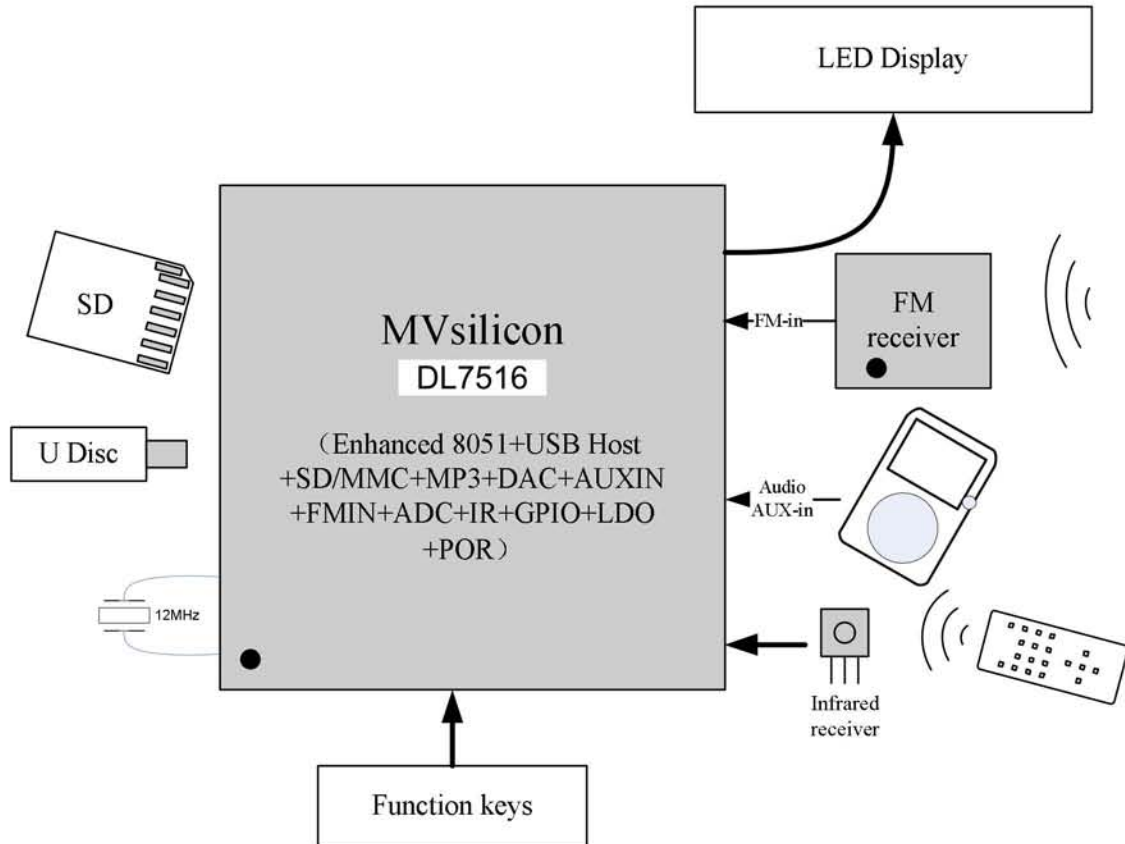


Figure 2 Mini Audio System



3. Pin Description

DL7516 is a CMOS device. Floating level on input signals causes unstable device operation and abnormal current consumption. Pull-up or Pull-down resistors should be used appropriately for input or bidirectional pins.

Notation	Description
I	Input
O	Output
I/O	Bidirectional
PWR	Power
GND	Ground

3.1 Pin Description

Table 1 Pin Description

Pin name	Pin #	Type	Description
USB interface pins			
USB_DP	27	I/O	USB Function D+ bus
USB_DM	26	I/O	USB Function D- bus
DAC interface pins			
DAC_R	12	AO	audio right channel output
DAC_L	13	AO	audio left channel output
DACVMID	11	AI	Internal voltage reference
DAC_AUX_R	14	AI	External AUX right channel in
DAC_AUX_L	15	AI	External AUX left channel in
GPIO/MCU IO pins			
GPIO_A[0]	7	I/O	GPIO PORT, bank A
GPIO_A[2]	25	I/O	GPIO PORT, bank A
GPIO_A[3]	22	I/O	GPIO PORT, bank A
GPIO_A[4]	24	I/O	GPIO PORT, bank A
GPIO_A[5]	23	I/O	GPIO PORT, bank A
GPIO_A[7:6]	17:16	I/O	GPIO PORT, bank A
GPIO_C[2]	8	I	GPIO PORT, bank C
GPIO_D[1:0]	21:20	I/O	GPIO PORT, bank D
GPIO_D[2]	5	I/O	GPIO PORT, bank D
GPIO_E[3:2]	18:19	I/O	GPIO PORT, bank E
CLK pins			
XIN	3	I	12MHz Crystal oscillator input for PLL
XOUT	4	O	12MHz Crystal oscillator output for PLL
Power/Ground pins			
DVSS	6	GND	ground for digital



DL7516 USB HOST MP3 DECODER SOC

LDO180	2	PWR	LDO 1.8V out
LDO330	28	PWR	LDO 3.3V out
LDO5V	1	PWR	LDO 5V power in
DACVDD33	9	PWR	power for DAC
DACVSS	10	GND	ground for DAC

4. Package

4.1 Package Diagram

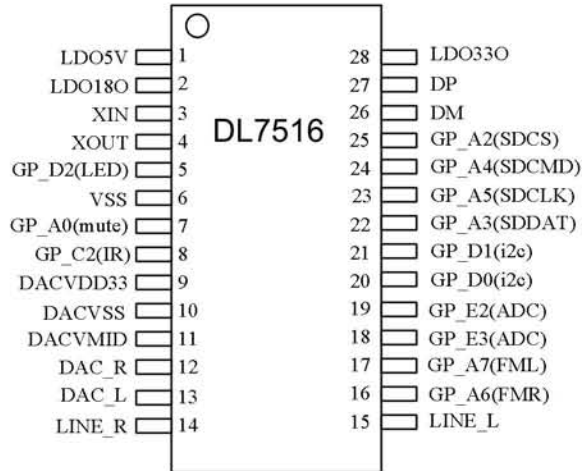


Figure 3 Package Diagram (SOP28 / TOP View)



4.2 Package Dimension Parameter

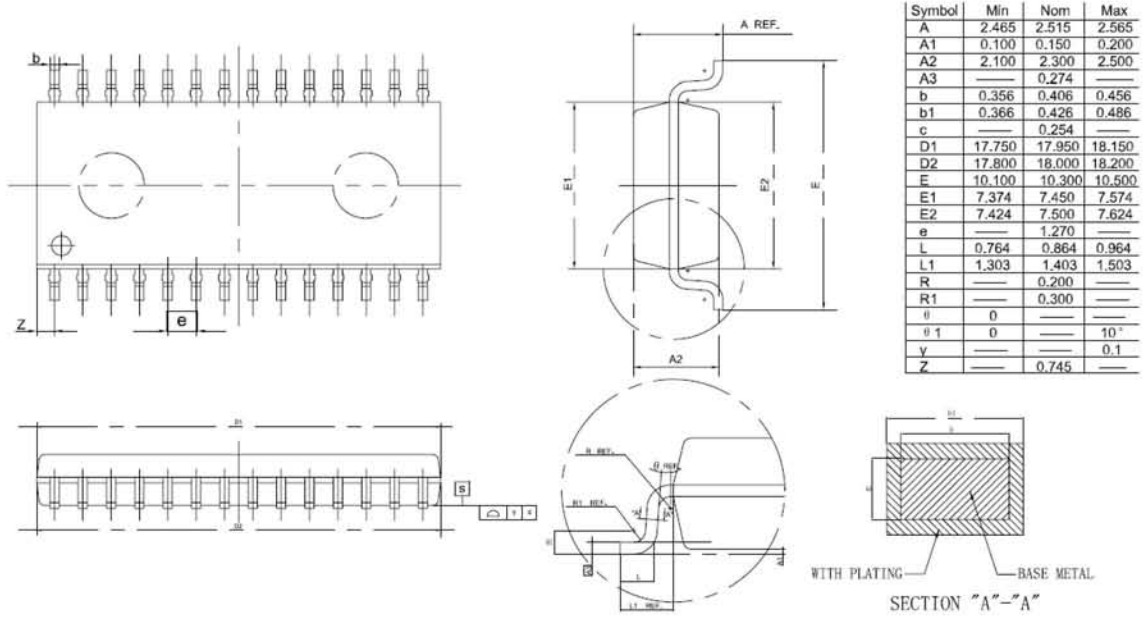


Figure 4 SOP28 Package Dimension Parameter



5. Electrical Specification

5.1 Absolute Maximum Ratings (Note 1)

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage (IO)	VCC_IO_AB	-0.5 to 4.6	V
Power Supply Voltage (Core)	VCC_CORE_AB	0 to 2	V
Storage Temperature	TEMP_STG	-65 to 150	C

5.2 Recommended Operating Conditions

Table 3 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (IO)	VCC_IO_OP	3	3.3	3.6	V
Power Supply Voltage (Core)	VCC_CORE_OP	1.62	1.8	1.98	V
Input Voltage (digital IO exclude GPIO C)	VIN	0		3.3	V
Input Voltage (GPIO C)	VIN	0		5	V
Operating Free Air Temperature	TEMP_OPR	-20		70	C

5.3 Electrical Characteristics

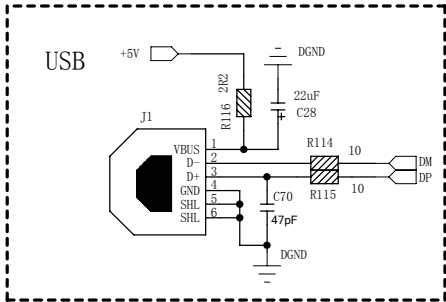
Table 4 Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIH	Input High Voltage		1.57		3.6	V
VIL	Input Low Voltage		-0.3		1.2	V
VOH	Output high voltage	@IOH=2mA	3.0			V
VOL	Output low voltage	@IOL=2mA			0.3	V
IL	Input leakage current		-10		10	uA
P_PLAY	Power consumption when playing	Playing mode		80		mW

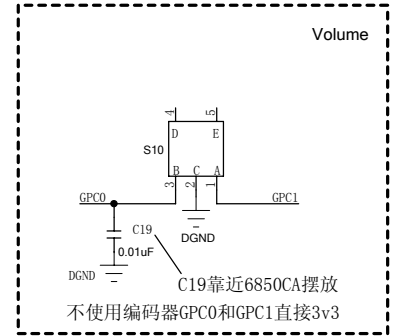
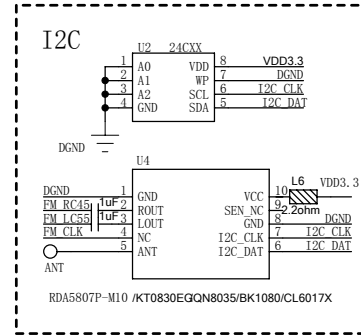
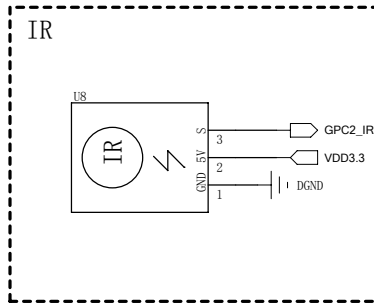
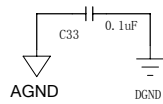
Note:

1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

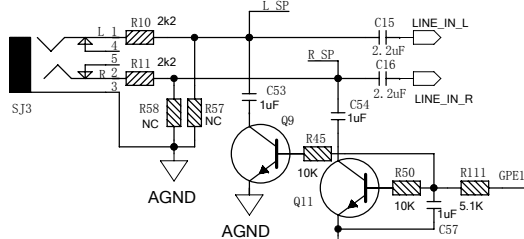
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C33 0.1uF电容请在靠近MCU AGND位置处增加



Line_in C15 C16电容改为>2.2uF可改善Line低频响应.



Line in输入电平必须<2.0V rms

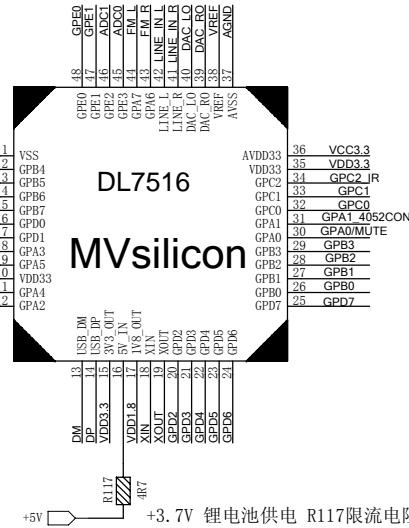
Line in&FM通道不使用时请悬空该通道PIN脚

如增加Q9 Q11 衰减网络, R111 C57 不能省略.

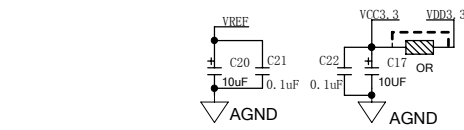
增加Q9/Q11电路是改善Line in对MP3/FM CH声音, 不加之电路测试Line in对FM/MP3 ch 衰减为>-70dB.

增加此电路测试Line in对FM/MP3 ch 衰减为>-80dB..由客户Option, 建议不加.

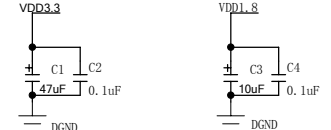
SD- CLK R27电阻短距离Layout设计可以省略



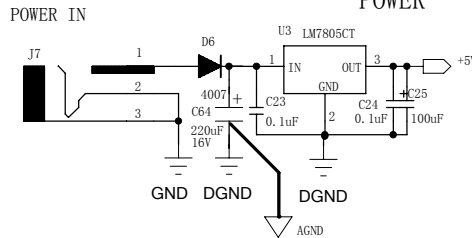
+5V 锂电池供电 R117限流电阻可以取消.



C20不能省略, Layout时靠近芯片引脚摆放.

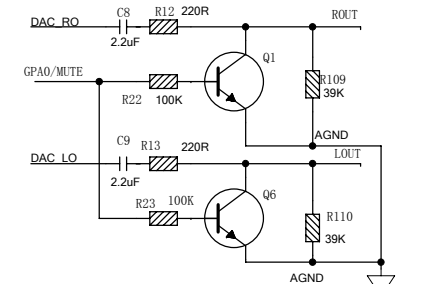


POWER

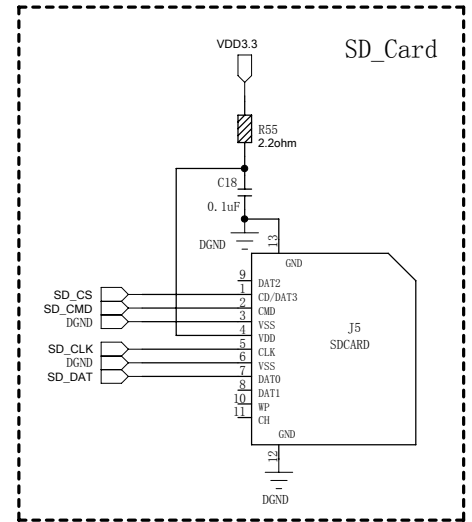
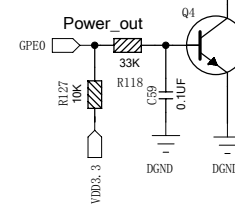


DGND与AGND必须在主板上POWER GND分开单点直接连通,

如果MP3音频信号是用电阻电位器做音量调节
需要在DAC输出增加R12, R13电阻做保护.



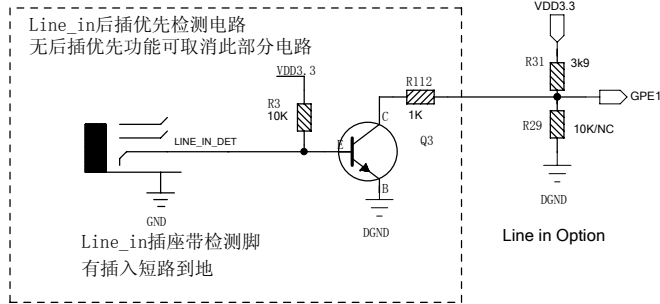
如果GPE0需要做power_control,
需要加上拉电阻10K到VDD33



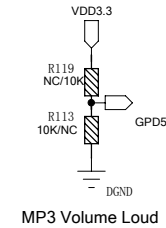
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APPROVED:	DATED:	PROJECT NO:	DRAWING NO:	
RELEASED:	DATED:	SIZE: A3	REV: V0.4	SHEET: 1 of 9

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无LINE_IN模式功能，只需保留R29电阻。其余Line in检测电路及Line in输入电路可省略

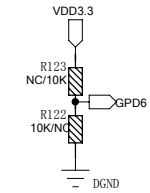


GPE1上拉1, 有LINE_IN模式
GPE1下拉0, 无LINE_IN模式
上拉或下拉电阻不能省略



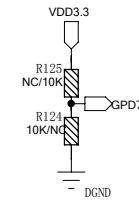
GPD5 Default Pull up MP3 输出幅度为680MV Rms 上拉电阻可以省略
GPD5 Pull Down MP3 输出幅度为1.1V Rms 下拉电阻不能省略

MP3 Volume Loud Option



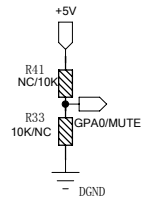
GPD6 Default Pull up FM搜台模式下DAC Clk off. 上拉电阻可以省略
GPD6 Pull down FM模式下DAC Clk off. 下拉电阻不能省略

DAC_CLK Option



GPD7 Default Pull up 上电默认EQ模式为Flat. 上拉电阻可以省略
GPD7 Pull down 上电默认EQ模式为Rock. 下拉电阻不能省略

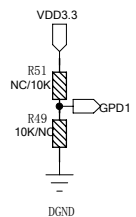
EQ_MODE Option



GPA0上拉1, 不记忆Standby.
GPA0下拉0, 记忆Standby模式

上拉或下拉电阻不能省略

Standby Memory Option



GPD1上拉1, FM使用32.768K时钟
GPD1下拉0, FM使用12MHz时钟

上拉或下拉电阻不能省略

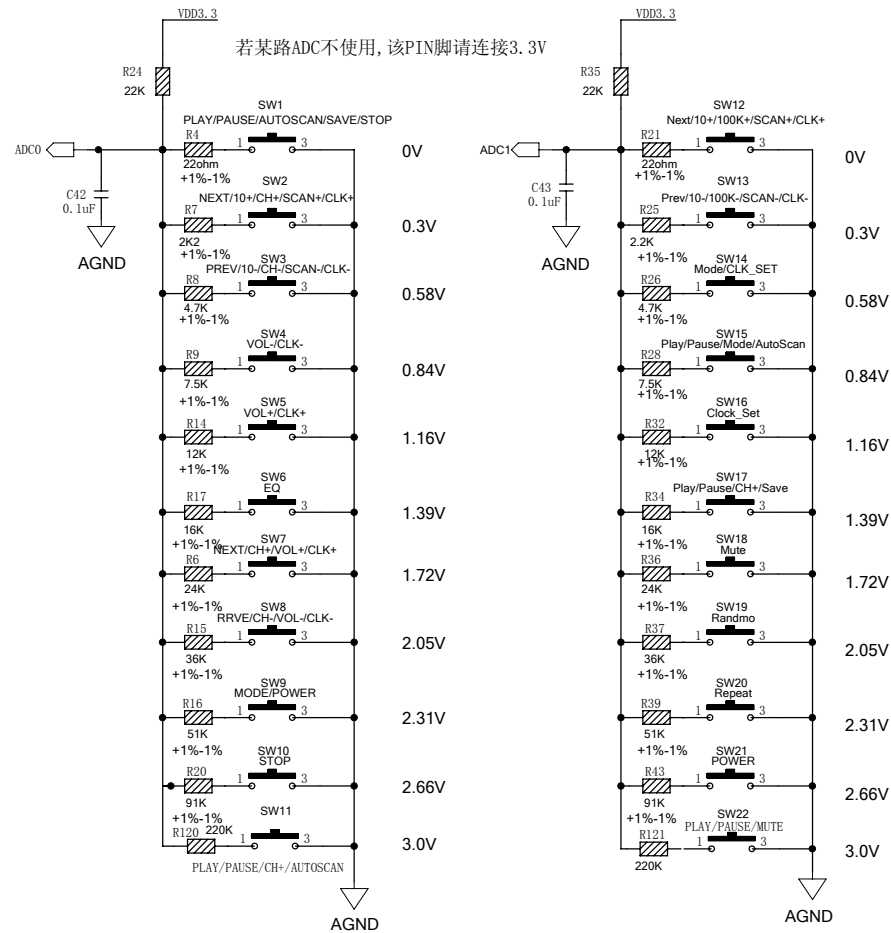
FM_CLK Option

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APPROVED:	DATED:	PROJECT NO:	DRAWING NO:	
RELEASED:	DATED:	SIZE: A3	REV: V0.4	SHEET: 2 of 9

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ADC 参考电压3.3V必须接芯片输出VDD3.3V

若某路ADC不使用, 该PIN脚请连接3.3V

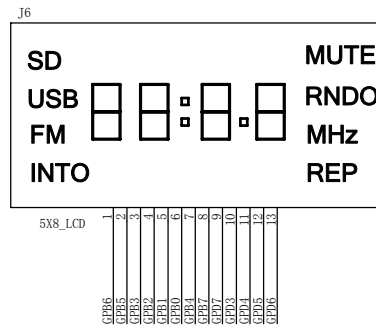
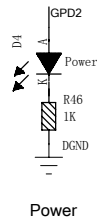


ADC KEY采集的地必须为AGND. 可以提高key的抗干扰能力.

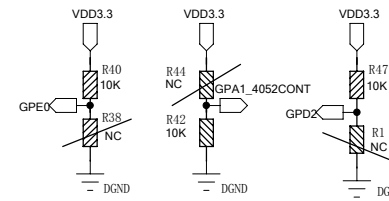
22 ohm电阻不能用0 ohm代替, 会影响系统稳定.

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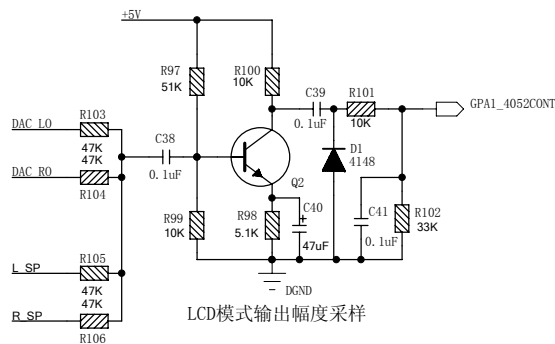


Mode0	Mode1	Mode2	显示模式
1	0	1	5X8_LCD



Mode0 Mode1 Mode2

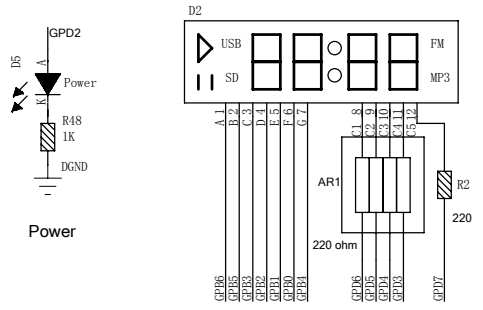
此模式如果有频谱采样电路R42可省略
 GPE0 默认 Pull up R40 可以省略
 GPA1 默认 Pull up
 GPD2 默认 Pull down R47须增加



LCD模式输出幅度采样

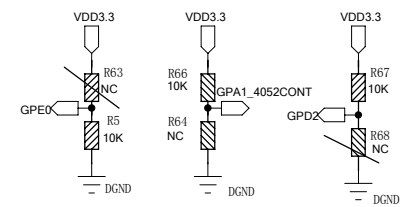
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RELEASED:	DATED:	SIZE: A3	REV: V0.4	SHEET: 4 of 9

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限流电阻放在seg端LED显示亮度更均匀

Mode0	Mode1	Mode2	显示模式
0	1	1	5X7数码管带时钟
0	0	1	5X7数码管不带时钟

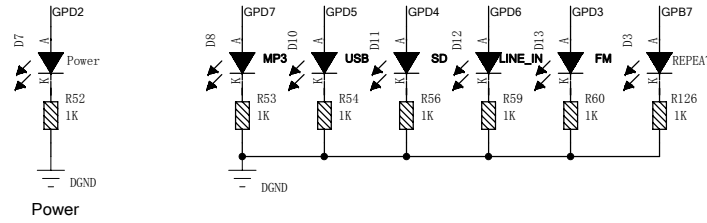


Mode0 Mode1 Mode2

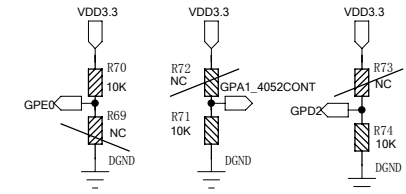
带时钟模式R66可省略, GPA1 默认Pull up
 不带时钟模式R64可省略, GPA1直接接地
 GPE0 默认 Pull up R5 须增加
 GPA1 默认 Pull up R66可省略
 GPD2 默认 Pull down R67须增加

DRAWN:	DATED:	COMPANY:		
CHECKED:	DATED:	TITLE:		
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RELEASED:	DATED:	SIZE: A3	REV: V0.4	SHEET: 5 of 9

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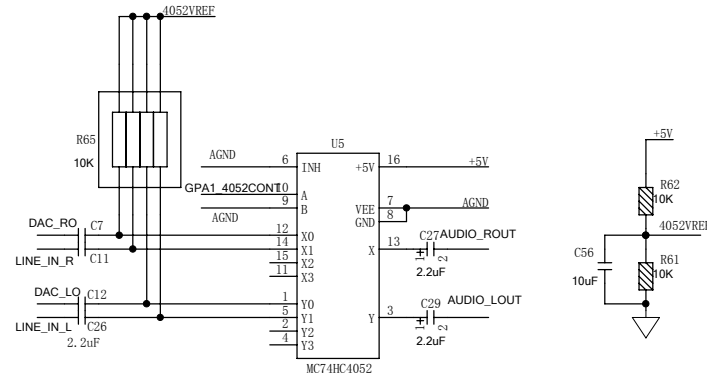


Mode0	Mode1	Mode2	显示模式
1	0	0	5个LED灯模式



Mode0 Mode1 Mode2

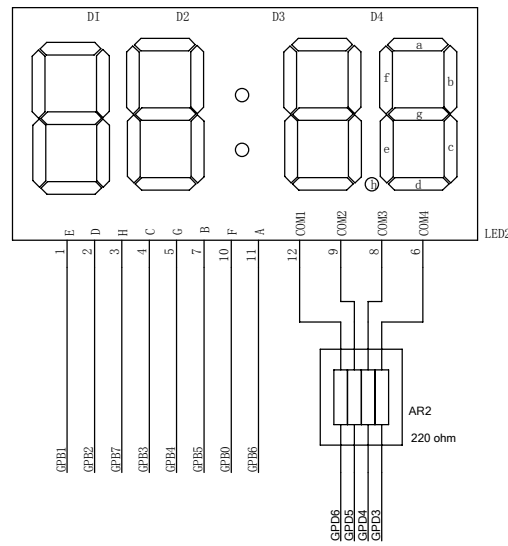
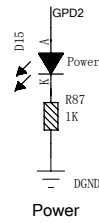
GPE0 默认 Pull up R70可以省略
 GPA1 默认 Pull up R71 需增加
 GPD2 默认 Pull down R74可以省略



针对大信号输入需求, 单独LED显示模式可以外加4052.

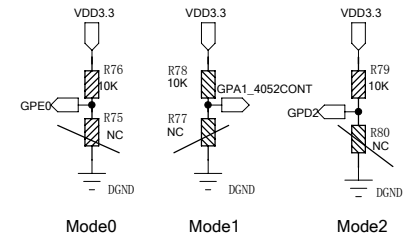
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RELEASED:	DATED:	SIZE: A3	REV: V0.4	SHEET: 6 of 9

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限流电阻放在seg端LED显示亮度更均匀

Mode0	Mode1	Mode2	显示模式
1	1	1	4个8带时钟

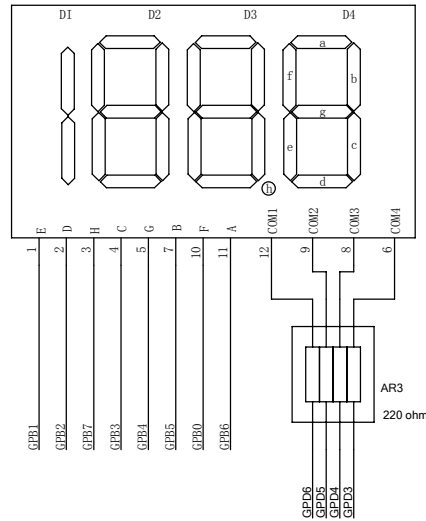
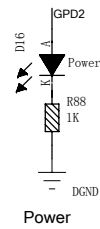


此模式R78可省略, GPA1直接接高

- GPE0 默认 Pull up R76可省略
- GPA1 默认 Pull up R78可省略
- GPD2 默认 Pull down R79 须增加

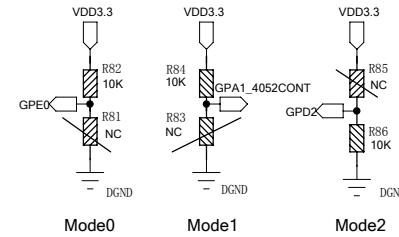
DRAWN:	DATED:	COMPANY:		
CHECKED:	DATED:	TITLE:		
APPROVED:	DATED:	PROJECT NO:	DRAWING NO:	
RELEASED:	DATED:	SIZE: A3	REV: V0.4	SHEET: 7 of 9

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限流电阻放在seg端LED显示亮度更均匀

Mode0	Mode1	Mode2	显示模式
1	1	0	3位半数码管

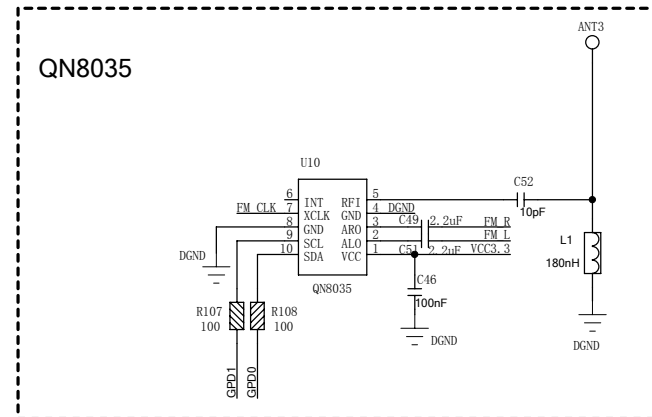
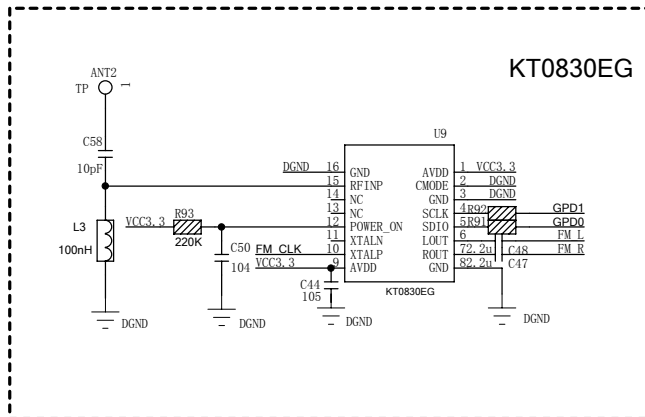
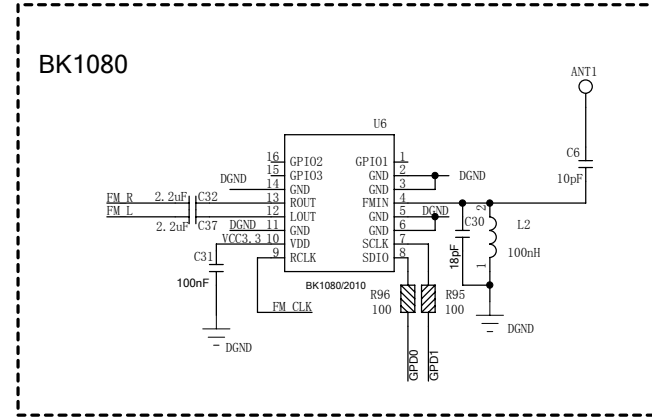
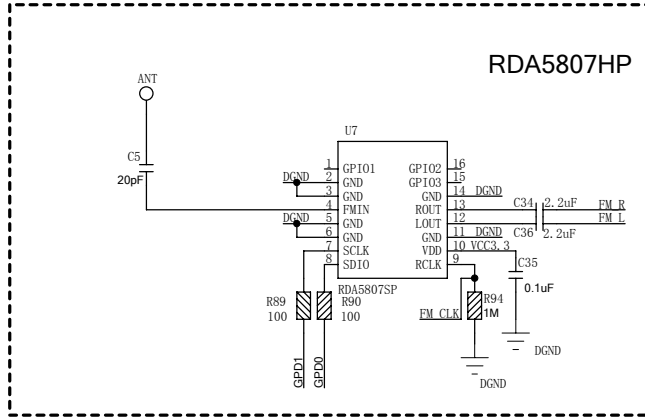


1888显示模式:

- GPE0 默认 Pull up R82可省略
- GPA1 默认 Pull up R84可省略
- GPD2 默认 Pull down R86可省略

DRAWN:	DATED:	COMPANY:		
CHECKED:	DATED:	TITLE:		
APPROVED:	DATED:	PROJECT NO:	DRAWING NO:	
RELEASED:	DATED:	SIZE: A3	REV: V0.4	SHEET: 8 of 9

Mountain View Silicon



DRAWN:	DATED:	COMPANY:		
CHECKED:	DATED:	TITLE:		
APPROVED:	DATED:	PROJECT NO:	DRAWING NO:	
RELEASED:	DATED:	SIZE: A3	REV: V0.4	SHEET: 9 of 9